REMARKS

Claims 10-20 are pending in the present application. Claims 18-20 have been presented herewith.

Claim Rejections-35 U.S.C. 103

Claims 10-17 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Capote et al. reference (U.S. Patent No. 6,297,560) in view of the Riding et al. reference (U.S. Patent No. 6,083,811). This rejection is respectfully traversed for the following reasons.

As emphasized in the Request for Reconsideration dated April 28, 2006, the Capote et al. reference as relied upon by the Examiner merely discloses a thickness of encapsulant material or sealing resin in a range of 50 to 200 μm. As acknowledged by the Examiner, the Capote et al. reference does not disclose the thickness of chip 10 shown in Fig. 4. Accordingly, the Capote et al. reference does not disclose or suggest a relationship between semiconductor element thickness and sealing resin thickness, and more particularly does not disclose such a relationship that would reduce the occurrence of cracks at a junction between a semiconductor element and a mounting substrate.

The Riding et al. reference as secondarily relied upon by the Examiner merely discloses that dice 20 has a thickness of about 100μm. The Riding et al. reference does not specifically show a sealing resin. Accordingly, the Riding et al. reference

clearly does not disclose or suggest a relationship between semiconductor element thickness and sealing resin thickness, and more particularly does not disclose such a relationship that would reduce the occurrence of cracks at a junction between a semiconductor element and a mounting substrate. The Riding et al. reference as secondarily relied upon by the Examiner thus fails to overcome the above noted deficiencies of the primarily relied upon Capote et al. reference.

The Zenner et al. reference (U.S. Patent No. 6,246,010) does not appear to disclose or consider a sealing resin in column 1, lines 14-20, as relied upon by the Examiner in support of this rejection. Accordingly, the Zenner et al. reference also fails to disclose or suggest a relationship between semiconductor element thickness and sealing resin thickness, and does not disclose such a relationship that would reduce the occurrence of cracks at a junction therebetween.

Accordingly, the prior art as relied upon by the Examiner, taken singularly or together, does not disclose or suggest a relationship between semiconductor element thickness and sealing resin thickness, as would be necessary to meet the features of claim 10.

On page 4 of the Final Office Action dated February 3, 2006, the Examiner has alleged that it would have been obvious to use the semiconductor element thickness teaching of the Riding et al. reference with the method of the Capote et al. reference in the range claimed, "because it is been held that where the general conditions of the claims are [disclosed] in the prior art, it is not inventive to discover the optimum or

workable range by routine experimentation".

However, contrary to the Examiner's assertion, the relied upon prior art does not disclose the "general conditions" of claim 10. The relied upon prior art discloses various thicknesses, but does not provide a specific teaching that cracks that occur primarily when mounting a semiconductor device on a substrate, can be sufficiently restrained by setting the thickness of the semiconductor element to 200 μm or less, and by setting the thickness of the resin to half or more the thickness of the semiconductor element. In absence of such a specific teaching disclosing this particular relationship, modification of the primarily relied upon prior art in the manner as suggested by the Examiner would appear to be based on impermissible hindsight. Applicants therefore respectfully submit that the method of mounting a semiconductor device on a mounting substrate of claim 10 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 10-17 is improper for at least these reasons.

With further regard to this rejection, claim 11 features that a thickness of a sealing resin on a peripheral portion of a semiconductor element that has a step part, is made to be greater than a thickness of the sealing resin on a central portion of the semiconductor element that is surrounded by the peripheral portion. The Examiner has asserted that these features are met by Fig. 11 of the Capote et al. reference.

However, as asserted beginning on page 6 of the Request for Reconsideration dated April 28, 2006, chip 10 (interpreted by the Examiner as the semiconductor

element of the claims) as shown in Fig. 11 of the Capote et al. reference does not have a step part. Element 39 in Fig. 11 is merely encapsulant material. Since chip 10 in Fig. 11 of the Capote et al. reference does not include a step part, the prior art as relied upon by the Examiner, particularly the Capote et al. reference, does not disclose or make obvious the features of claim 11. Applicants therefore respectfully submit that claim 11 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claim 11 is improper for at least these additional reasons. **If this rejection is to be maintained, the Examiner is respectfully requested to identify on the record how chip 10 in Fig. 11 of the Capote et al. reference may be interpreted as having a step part.**

Claims 18-20

Applicants respectfully submit that claims 18-20, as dependent upon claim 10, distinguish over and would not have been obvious in view of the prior art as relied upon by the Examiner for at least the reasons as set forth above, and by further reason of the features therein.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejection, and to pass the claims of the present application to issue, for at least the above reasons.

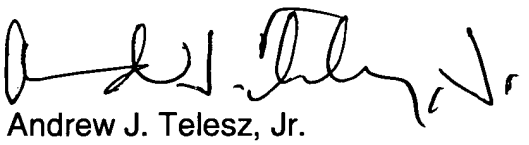
In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicants hereby petition for an extension of one (1) month to June 3, 2006, for the period in which to file a response to the outstanding Office Action. The required fee of $120.00 should be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



Andrew J. Telesz, Jr.
Registration No. 33,581

One Freedom Square
11951 Freedom Drive, Suite 1260
Reston, Virginia 20190
Telephone No.: (571) 283-0720
Facsimile No.: (571) 283-0740